Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0003D1	Serial No.: 10/661,037
Information Disclosure Statement by Applicant	Applicant: John D. Hyde et al.	
(Use several sheets if necessary)	Filed: September 12, 2003 Group: 2822	

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
	A	2003/0206437	11/6/2003	Diorio et al.	365	185.03	
	B	2004/0004861	1/5/2004	Srinivas et al.	365	185.21	
	C	2004/0021166	2/5/2004	Hyde et al.	257	314	
	D	2004/0037127	2/26/2004	Lindhorst et al.	365	202	
	E	2004/0052113	3/18/2004	Diorio et al.	365	185.21	
	F	5,627,392	5/6/1997	Diorio et al.	257	315	
	G	5,633,518	5/27/1997	Broze	257	314	
	H	5,666,118	9/9/1997	Gersbach	341	120	
	I	5,666,307	9/9/1997	Chang	365	185.03	
	J	5,687,118	11/11/1997	Chang	365	185.19	
	K	5,691,939	11/25/1997	Chang et al.	365	185.18	
	L	5,706,227	1/6/1998	Chang et al.	365	185.18	
	M	5,736,764	4/7/1998	Chang	257	318	
	N	5,841,165	11/24/1998	Chang et al.	257	318	
	O	5,875,126	2/23/1999	Minch et al.	365	185.01	

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No
	P	0 776 049	5/28/1997	EP			X	
	Q	0 778 623	07/18/2001	EP			X	

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	R	Chang, et al., "A CMOS-Compatible Single-Poly Cell for Use as Non- Volatile Memory", International Semiconductor Device Date Research Symposium, December 1-3, 1999.
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	T	Chung, et al., "N-Channel Versus P- Channel Flash EEPROM-Which One Has Better Reliabilities", IEEE Annual International Reliability, 2001, pp. 67-72.
	U	Declercq, et al., "Design and Optimization of High-Voltage CMOS Devices Compatible with a Standard 5 V CMOS Technology", IEEE Custom Integrated Circuits Conference, 1993, pp. 24.6.1-24.6.4
	V	Diorio, et al., "Adaptive CMOS: From Biological Inspiration to Systems-on-a-Chip"; IEEE, Vol 90, No. 3; March 2002; pp 345-357.
	W	Diorio, et al., "A Floating-Gate MOS Learning Array with Locally Computed Weight Updates" IEEE Transactions on Electron Devices, vol. 44, No. 12, December 1997, pp. 1-10.

Examiner [signature] Date Considered 6-24-05

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

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Init.		Document No.	Date	Name	Class	Subclass	Filing Date
KA	X	5,898,613	4/27/1999	Diorio et al.	365	185.03	
	Y	5,912,842	6/15/1999	Chang et al.	365	185.11	
	Z	5,914,894	6/22/1999	Diorio et al.	365	185.03	
	AA	5,966,329	10/12/1999	Hsu et al.	365	185.18	
	AB	5,986,927	11/16/1999	Minch et al.	365	185.01	
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	AD	6,055,185	4/25/2000	Kalnitsky et al.	365	185.18	
	AE	6,081,451	6/27/2000	Kalnitsky et al.	365	185.18	
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	AJ	6,166,954	12/26/2000	Chern	365	185.14	
	AK	6,190,968	2/20/2001	Kalnitsky et al.	438	259	
KA	AL	6,208,557	3/27/2001	Bergemont et al.	365	185.15	

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KA	AM	Diorio, et al., "A High-Resolution Non-Volatile Analog Memory Cell", IEEE, 1995, pp. 2233-2236.
	AN	Diorio, "A p-Channel MOS Synapse Transistor with Self-Convergent Memory Writes", IEEE Transaction On Electron Devices, Vol. 47, No. 2, pp. 464-472, February 2000.
	AO	Hasler, et al., "An Autozeroing Amplifier Using PFET Hot-Electron Injection", IEEE, 1996.
	AP	Hasler, et al., "Single Transistor Learning Synapses", Cambridge, MA, The MIT Press, 1995, pp. 817-824.
	AQ	Hasler, et al., "Single Transistor Learning Synapse with Long Term Storage", IEEE, 1995, pp. 1660-1663.
KA	AR	Hasler, et al., "An autozeroing Floating-Gate Amplifier", IEEE Transactions on Circuits and Systems, Analog and Digital Signal Processing, Vol. 48, No. 1, January 2001, pp. 74-82.

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Init.		Document No.	Date	Name	Class	Subclass	Filing Date
	AS	6,222,771	4/24/2001	Tang et al.	365	185.22	
	AT	6,452,835	9/17/2002	Diorio et al.	365	185.03	
	AU	6,479,863	11/12/2002	Caywood	257	321	
	AV	6,534,816	5/18/2003	Caywood	257	314	

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Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	Hyde, et al.; "A Floating-Gate Trimmed, 14-Bit, 250 Ms/s Digital-to-Analog Converter in Standard 0.25 um CMOS", Impinj, 2002 Symposium on VLSI Circuits, Honolulu HI; pp 328-331.

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